Curriculum Vitae

Mob: 8295621664,9876325430

rajeevpundir@hotmail.com

Objective

Working in real time projects in VLSI Design and enhance my knowledge and skills so that I am finally stand in parallel in latest technology.

Professional Qualification

Degree	Uni/Board	Percentage	Year	Specialization	Status
M.Tech	KUK	71.92	2011	Microelect & VLSI Design	Completed
MSc	KUK	63.6	2007	Electronic Science	Completed
BSc	UP Board	64.6	2005	Electronics	Completed

Languages Known

Chip Design

Verilog HDL

VHDL

Software

C Language

System Platform

Operating System	Name
Windows	XP,NT,2000,7
Linux	Redhat,Fedora,Sunsolaris

EDA Tools

Field	**Name**
Digital Design	Modelsim 6.4a,HDS,FPGA Advantage, Active HDL 6.3,7.2
Analog & Mixed Signal Design	Winspice,Multisim,IC Station,Eldo
Process Simulation	Atlas,Athena,Icrcrem
Synthesis	Xilinx,Precision,Leonardo Spectrum
Signal Processing	Matlab 6.1

Subjects Known:

Analog Design

Digital Design

IC Fabrication Technology

Microwave

Microprocessor

Microcontroller

Processor Design

C Language

Verilog HDL

VHDL

Analog Communication

Opamp

Projects:

MSC Electronic Science

Field	***Details***
Thin Film Deposition	Aluminum Titanium

Pattern Transfer	UV Lithography 365-415nm Wavelength
Wet Etching	Etching of SiO_2 Etching of Si_3N_4 Etching of Aluminum Etching of Titanium Anisotropic Etching of Si

M.Tech MMVD (FPGA Based Prototyping)

Tool:

Simulation: Modelsim, HDS, FPGA Advantage

Synthesis: Xilinx ISE 10, 10.1

Verilog HDL (RTL Coding)

Design of Reconfigurable VLIW Processor

Design of RISC Microcontroller

Design of Moore Machine

Design of Seven Segment Decoder

Design of JK, D, TFF

Design of 64bit Program Counter

Design of RAM

Design of ROM

Design of CMOS Inverter, NAND, NOR Gate using transistor level design

Design of Ripple Counter

Design of Full Adder

Design of 32bit Floating Point Multiplier on FPGA

VHDL

Design of Half Adder, Full Adder

Design of 2*4 line Decoder

Clock constant time, variable time period

Design of Mealy Machine

FPGA Prototyping

Design tested on Spartan2 FPGA using xc2s200fg256 device with speed grade -6.

Full Custom Design

Tool:

IC Station (Design Architect) run in Redhat Linux

CMOS Inverter Design based on 0.1µm Technology

NMOS Inverter Design based on 0.1µm Technology

Design of Differential Amplifier based on 0.1 µm CMOS Technology

Analog & Mixed Signal Design

Tool: Winspice, Multisim, Eldo

Passive RC Filters

Active Filters (Low Pass, High Pass, Band Pass, Band Reject)

Design of Common Emitter Amplifier using BJT **BC107 (NPN Transistor)**

Process Simulation

Tool: Atlas, Athena

Design of 0.1 µm NMOS

Tool: Icecrem

Oxidation, Etching, Epitaxy

DSP

Tool: Matlab 6.1

Solution of Various Mathematical Equations

Curve Tracing

BSc Electronics

Regulated Power Supply

Running Light

Professional Experience

Teaching: Three Years

Research: 1 Year

Papers Published: 12

Field	**No.**
Microelectronics	1
VLSI Design	9
DSP	2

Membership

Member of International Association of Engineers (IAENG)

Membership No: 121529

Member of IACSIT

Membership No:80345696

Reviewer of Global Journal Inc. (USA, UK)

Member of Research Gates

Member of Silicon India

Conference Attended:

IMS during 17-19 February 2006 in KUK

AMS during 21-22 February 2010 KUK

Seminar Delivered

Formal Verification in ASIC Design

CMOS Technology

Materials for LED

Process Optimization for Photolithography

Gyrotron Technology

Data Types in VHDL

Porous Silicon

Design of Reconfigurable VLIW Processor

Area of Interest

Name	***Field***
High Performance VLSI Architecture	VLSI Design
Low Power VLSI Design	VLSI Design
ASIP Architecture for High Performance & Low Power	VLSI Design

Achievements

1.	Worked on Anisotropic Etching during MSc Electronic Science
2.	Worked on Advanced Processor Architecture during M.Tech (Microelectronics & VLSI Design) VLIW Processor
3.	Currently working in ASIP Design & Implementation (Advanced Processor Architecture)
4.	Participated in AMS Conference during 21-22 Feb 2010 KUK

Future Work

Design & implementation of ASIP for High Performance on FPGA

Design of 64bit DSP Processor for H.264

Design of UART for High Speed & Low Power on FPGA

Currently working on Design of RISP Processor Architecture based on 65nm CMOS Technology

Project Completed

Design of Signed/Unsigned Multiplier on FPGA

Comparison of Gate Count, Power & Delay in 64 bit Adder, Subtractor & Multiplier

Comparison of Area/Power in 1's, 2's & 9's Complement System

Design & Implementation of Execution Unit for 32 bit ASIP Processor Architecture for High Performance

Simulation Study of Astable Multivibrator Complexity Analysis in Wave Generator

Design & Implementation of ASIP & Code Generation on FPGA for High Performance

Paper Published

International Journal-12

National Journal-Nil

S.No.	Title	Journal
1	Design of 64 bit Integer Multiplier for Low Power Consumption	IJERA
2	Design of High Speed Variable Width Integer Multiplier	IJERA
3	Design of 64 bit Register File for VLIW Processor Architecture	IJERA
4	Design of high performance & low power up down counter on FPGA	IJERA
5	Impact of Architecture Design on Area & Clock Latency in Hardware Design	IJVSPA
6	Design & Implementation of Instruction Memory for ISA & tradeoff between Speed/Power Consumption	IJVSPA
7	Design & implementation of 64 bit ALU for ISA & comparison between speed and power consumption on	IJARCET

	FPGA	
8	Etching of Metallic & Dielectric films in VLSI Technology	IJARCET
9	Design of Wideband Inset feed Microstrip Patch antenna for wireless applications	IJEST
10	Design of Variable Width Barrel Shifter for High Speed Processor Architecture	IJEST
11	Design & Implementation of Majority Gates on FPGA & Comparison of Area/Power tradeoff	IJEST
12	Optimal Design RRC Pulse Shape Polyphase FIR Decimation Filter for Multi-Standard Wireless Transceivers	IJARCET

Work Experience:

1µm NMOS Technology

0.1µm CMOS Technology

90nm CMOS Technology

65nm CMOS Technology

Personal Details

Name: Rajeev Kumar

Father's Name: Sh.Jung Singh

DOB: 18/02/1984

Address: Shiv Puri B Colony, YNR-135001(HR)

Mobile: 8295621664, 09876325430

Marital Status: Single

Email:rajeevpundir@hotmail.com,transistor.bjt@gmail.com,transistor@rediffmail.com

Ref:

Dr.Mukesh Kumar

Assistant Professor Deptt of Electronic Science, KUK

kumarmukesh@gmail.com

Dr.P.J George

Director/Principal KITM, Kurukshetra

pjgeorge@hotmail.com

Declaration

I hereby declare that the above information is true to best of my knowledge and belief.

Date:

Place:

Rajeev Kumar