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An Implementation & Analysis Pipeline Analog to Digital Converter Comparator Based Performance By Threshold inverter quantization (TIQ)

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***Abstract*— Demand for high-performance analog-to-digital converter (ADC) integrated circuits (ICs) with optimal combined specifications of resolution, sampling rate and power consumption becomes dominant due to emerging applications in wireless communications, broad band transceivers, digital-intermediate frequency (IF) receivers and countless of digital devices. This research is dedicated to develop a pipeline ADC design methodology with minimum power dissipation, while keeping relatively high speed and high resolution. A 14-bit pipelined analog-to digital converter (ADC) is designed in this work. The pipelined architecture realizes the high-speed and high-resolution. To reduce some complexities of flash ADC pipeline ADC is used. The calibration schemes of pipelined ADC limit absolute and relative accuracy. This paper illustrates a 14 bit 80-Megabit sample/s ADC made-up in a 0.18 micrometer CMOS technology. The converter employs pipelined seven stages and implement 2 bit per stage by using 0.18 CMOS technology.**

IndexTerms - Analog-To-Digital Converter (ADC), Integrated Circuits (Ics), Micrometer CMOS and Active Area Gate Oxide Width (Cox)

I. INTRODUCTION

For ADCs with resolutions of 8 to 14 bits and sample speeds ranging from a few MS/s to hundreds of MS/s, the pipelined topology is a popular alternative. When compared to other Nyquist-rate data converters such as Flash, folding interpolating, and so on, the topology's popularity can be attributed to its relatively simple and repetitive interior configuration, as well as a significant reduction in the number of comparators required to achieve a fixed resolution. Mobile systems, CCD imaging, ultrasonic medical imaging, digital receivers, pedestal stations, digital video (e.g., HDTV), x DSL, cable modems, and fast Ethernet are just a few of the applications that pipelined ADCs are employed in [1].With the use of pipelined ADCs in many consumer products, research in improving the performance of pipelined ADCs has attracted much attention in excess of the long-ago decade, where the largest part accepted areas of explore have been: linearity enhancement, and power reduction. Because of the low intrinsic gain, low supply voltages, and device mismatch found in deeper sub-micron technologies, creating very linear data converters (i.e. >10-bit linear) utilizing traditional pipelined ADC design methodologies has been a focus of research. Low power consumption in pipelined ADCs is driven by the fact that pipelined ADCs are used in many mobile devices, where low power consumption allows for longer battery life and hence greater consumer efficiency. In agitated systems wherever many ADCs are able to be integrated on-chip in equivalent, huge net supremacy expenditure can spawn high amounts of heat requiring expensive packaging for heat dissipation. Analog vs. Digital Information: Analog signals have an infinite number of output states, whereas digital outputs only have a finite number.

Fig.1.1 **Example of An Analog Signal**

II. LITERATURE REVIEW

Due to the widespread usage of PCM (Pulse Code Modulation) technology in the telecommunications industry, ADC was initially increased in the 1930s. It changed the analog coding and decoding technology into digital signal processing technologyADC received continued development until the 1950s, when high-speed digital computers and aircraft/missile data processing systems were introduced. After Microprocessors were well-developed in 1970s, it triggered a technological revolution in the field of digital signal processing and computer. In 1971, the first Monolithic ADC was designed as analog/digital interface circuitry. Deep sub-micron integrated technology has been more widespread in the last 20 years, promoting a new area of analogue integrated circuits: mixed signal integrated circuits. This chapter will provide a brief overview of all common ADCs, including flash ADCs, two-step ADCs, pipeline ADCs, and so on.

To bias Buckel Peter Preyler Alexander KlinkanDamir Hamidovic Christoph Preissl Thomas Mayer Stefan Tertinek Siegfried Brandstaetter Christian Wicpalek Andreas Springer Robert Weigel A Novel Digital-Intensive Hybrid Polar-I/Q RF Transmitter Architecture IEEE Transactions on Circuits and Systems Proposed hybrid digital transmitter (TX) transmitter system, combining traditional phase and quadrature (I/Q) with limited time distortion. The proposed architecture uses an RF-DAC with an RF clock frequency and modified I / Q components. By mixing the phase changes, the quadrature element is kept small, while the internal element is close to the complex signaling envelope. Compared to the TX quadrature digital architecture, it results in a significant reduction in the RF-DAC field. Therefore, RF-DAC can work with less deterioration in high output power and water efficiency. The modification of the process is limited to suspend the requirements of the modulator system. Compared to the TX polar digital architecture that uses a rotating digital RF communication channel with two-phase processing, the digitally controlled oscillator reduces the requirements for climate change and control parameters. In addition, the design work has shifted more and more from the analog field to the digital field to take full advantage of the unique advantages of CMOS technology.

Pummy Ratna Usha P Verma Enhanced Receiver Architecture For Leakage Reduction in Wideband EW Transceivers With Overlapping RF And IF EW transceivers have high-frequency, wide-angle communication channels and RF and IF communication channels that overlap andare used to detect and detect input signals, and are sensitive to RF and LO in IF, which can lead to Leak misrepresentation and use traditional methods to use Spurs as a threat signal. This article presents a redesigned design that has been successfully used in the radio frequency portion of afree channel digital transceiver to accurately detect threat signals by modifying the channel used. all to X-band and the low conversion to IF. This eliminates the direct problems of water leakage and leakage inhibition and the isolation requirements of the mixer for image and false pressure, and provides a low impurity signal for low-IF Nyquist samples. in many introductory areas. The system was successful in testing the -60dBm false positives, RF and leakage levels of the dense pulse-input signal in the -10 to -50dBm range. The improved structure, test results and comparison of the results of the heterodyne structure were included.

Ram Sunil Kanumalli Ahmed Elmaghraby Andreas Gebhard Christian Motz Thomas Paireder ; Christina Auer Mario Huemer Mixed Signal Based Enhanced Widely Linear Cancellation of Modulated Spur Interference in LTE-CA Transceivers 2018 Implementing a combination transceiver (CA) on a mobile phone can result in unnecessary manipulation of the frequency transceiver (RF) chip. In common duplex distribution mode (FDD), this can cause a decrease intrans mission leakage (TX) in one of the receivers, resulting in sensory interference. When a cell phone is operating at the edge of a cell, this interference can impair the reception efficiency (RX).The recent mixed signal elimination technique that is proposed refers to the use of receivers to detect TX leakage signals. When there is an imbalance of IQ in the path of help, the reference signal obtained from the input of digital cancellation will be contaminated by its characteristic elements. This limits the performance of the multi -dimensional architectural design that aims to eliminate image and image distortion techniques. In this article, we propose a more comprehensive abstraction model that digs the image elements into the label, which improves the abrasion performance. The performance of the elimination structure is verified by the design of the system.

T. Buckel P. Preyler E. Hager T. Mayer S. Tertinek A. Springer R. Weigel A Novel Hybrid Polar-I/Q Modulation Method relaxing RF Phase Modulator Design Requirements 2018 proposed a data processing project that combines in-phase / quadrature (I / Q) and phase modulation to achieve a powerful digital quadrature and polar transmitter architecture. An endless transition between them. With the timing, the peak power rating of the input code of the digital-to-analog converter (DAC) is reduced. Therefore, the RF-DAC quadrature can operate in the low return region, resulting in high power output and drain efficiency. The simulation results of the LTE traffic signal are presented, including a new manipulation strategy that combines a channel efficiency model with a common cell and an RF-DAC that is inverted. Compared with digital quadrature transmitters, the output power and efficiency can be improved, close to the digital polarity limit, and greatly reduce the requirements on the phase modulation path.

Seok-Ju Yun Jaechun Lee Joonseong Kang Chisung Bae ;Junyeub Suh Sang Joon Kim A Low Power Fully Intergrated RF Transceiver for Medical Implant Communication 2018 IEEE International Symposium on Circuits and Systems (ISCAS) Year: 2018 This article

presents a fully integrated RF transceiver with small size and minimum power performance. The transceiver is implemented by using an LC oscillator with a frequency antenna on the radio as the input element. The proposed receiver converts the time to start the oscillation in response to the OOK signal used as a digital output. The sophisticated transceiver allows for optimal size and power efficiency through Class C operation. The transceiver is made of 0.18 µm CMOS. The transceiver achieves 32.2% transmitter efficiency below -28.5 dBm EIRP, while consuming 2.2 mW and - 85 dBm receiver sensitivity in 25 kbps OOK input. In an experiment that mimics human – induced conditions, the transceiver is connected to an external base station with 1m of cordless wires and 8cm of implantation depth.

III. PROPOSED MODIFIED

Since the penetration should be as soon as possible, every phase of the pipeline ADC form is inherited Flash construction. The resolution of the individual steps will decide how many comparators are adjusted, which will be the latency of the structure, what type of DAC architecture must be necessary for the fast coding circuits. For preamble when we decide for 3 bits per phase, then 7-bit pipeline ADC, which for, will be there a total of three phases that you have a bit of ADC and has remaining 3-bit ADC architecture, so The fact that the total number of comparator required SO 35 (23 + 23 + 12) is also two (2 bits) and a (1 bit) DAC required. Since the selected architecture exists from one bit ADC, it is only a comparator required, and the total number of comparator 7 is reduced radically this is the motivation that simplifies the design of other sub-blocks from each phase, for example DAC design and associated digital Circuits. Figure 3.1 shows architecture of each pipeline phase ADCfor the design of each phase of the pipeline ADC (shown in Figure 3.1), wherein the required components.

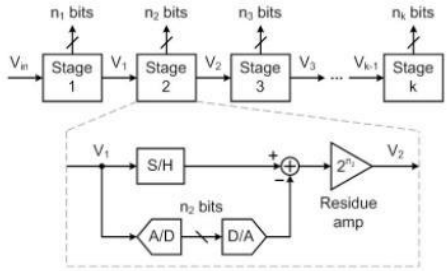

Fig 3.1 Single stage pipelined

3.1 DESIGN OF COMPARATOR

Implemented Flash ADC contains the TIQ technology (TIQ) technology (TIQ) for high-speed and low-power ADC with standard CMOS technology. Displays the block diagram of the qunatizer comparator of the threshold value. The use of cascade inverters simultaneously with a voltage comparison is the reason for the name of the method. The voltage comparators measure on the input voltage with internal reference voltages searching by the dimensions of the transistor. Some number the most important problems of the usual structure comparator in ADC designs are used are:

I. Large transistor surface for higher accuracy,
II. DC bias request,
III. Injection errors,
IV. Met stability Error, High flow consumption, resistance or condenser ATRIX

This case would be necessary to integrate BICMOS technology to integrate both high-speed conversion and low-power derivation. The proposed comparator has been described in this work, not only developed for a higher speed, but also for a higher resolution.

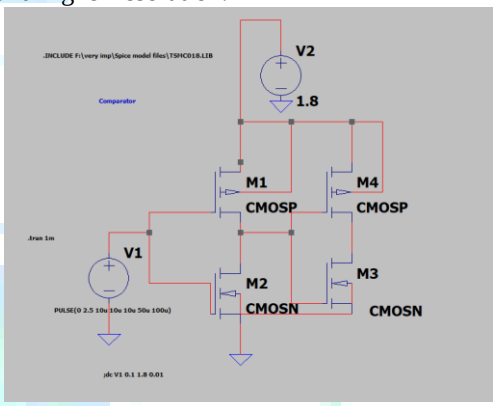

Figure 3.2 Schematic of Comparator

Design:

We have contained that both transistors are in the active area gate oxide width (Cox) for both transistors is the same, or lengths of both transistors (Lp and Ln) are also the same.

Expanding equation

$$V_t = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\left(V_{dd} - V_{tp}\right) + V_{tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

Wherever, µp and µn are the electron and hole mobility.

Since, in projected architecture three comparator are requisite. So we have to propose three comparator to get their threshold voltages we need to calculate Width & Length.

3.2 DESIGN OF TWO BIT DAC

There are different configurations that can be used to design a digital-to-analog converter (DAC), similar to a resistor hierarchy (voltage divider architecture), charge sharing principles, current sharing architecture, and more, but they all involve many components and complexity in nature. So, in CMOS digital technology, the multiplexer logic was used as a DAC because the purpose of the DAC is to provide an analog voltage corresponding to the digital bits as shown in Table 4.3. This means that an analog multiplexer can handle this task with ease. the logic equation repeats the procedure of the multiplexer we use here as

2DAC. $Z = A(S1.S2)+B(S1.\overline{S2})+C(\overline{S1}.S2)+D(\overline{S1}.\overline{S2})$

Figure 3.3 shows an analog multiplexer circuit, the multiplexer has many inputs and only one output, so in the proposed work each stage consists of 2 bits, so a 4: 1 multiplexer is required the operation looks like this - if "S0 S1" is zero , then M1 and M2 are on, so "Vref1" is transmitted, and we get an analog value of 0 V. If S1 = 0, S = 1, then transistors M3 and M4 are on, so Vref2 after passing, we get an analog value of 0.045 V , if S1 = 1, S2 = 0, then M2 and M5 are on, so after setting "Vref3" we get an analog value of 0.9 V. If S1 = 1, S2 = 2, then M4 and M6 are on, therefore "Vref4" transmitted. then we get an analog value of 1.355V The reference voltages are generated by a simple resistor divider circuit with two power supplies at each end of the resistor divider, which works in a similar way to an active ladder network. The drain is connected to the gate, and the source is connected to the substrate. The reference voltages are generated using a simple resistor divider circuit with two power supplies at each end of the resistor divider.

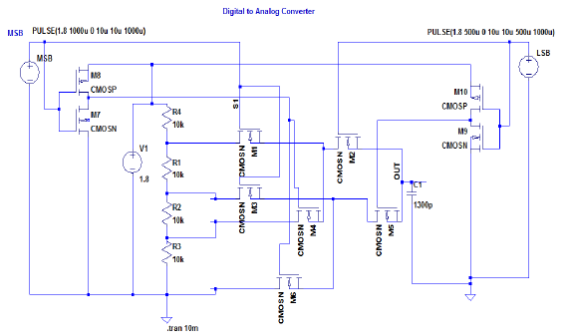

Fig 3.3 Schematic of 2-Bit DAC

That has similar works, such. An active conductor network, the active resistance is a moss connected in the diode configuration, d. H. DRAIN is connected to the substrate with port and source. The intention of this powerful resistance network depends on the given electricity and area restrictions. Like VGS = VDS Each MOSFET is activated in the saturation area and the resistance is set.

3.3 SAMPLE & HOLD CIRCUIT

Sample and hold circuits are required for the ADC's front-end circuitry to allow the ADC to track and then maintain the signal coming in. (See [8] for the sample-and-hold circuit argument.) After tracing the signal, the ADC turns on the switch to disconnect the input signal from the external interface; then maintains this input level for a long time. Enough to complete the ADC conversion cycle. These sample and hold or T / H circuits have significant bandwidth to allow the ADC to track the high frequencies of the input signal. They must remain linear across the entire bandwidth, which requires excellent design techniques to provide high bandwidth without adding unnecessary interference. The switching and conduction of the capacitors must charge and maintain the presentation of the signal over an extended period of time to allow the ADC quantizer to accurately estimate the change in amplitude of the input signal over its duration.

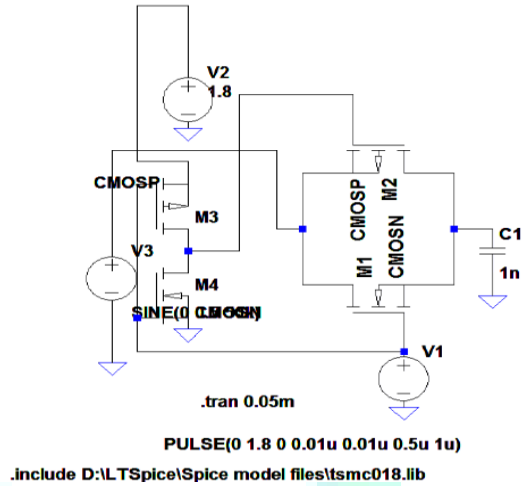

Figure 3.4 Schematic of Sample & Hold Circuit

The CLK sampling is known to the TX port. When the CLK is high, the input signal from left to the side is sampled, the 1st buffer and the capacitor are charged at the input level. If, as soon as the CLK goes too low, the path of the input is opened and the sampled voltage is reserved constant and specified the previous block for conversion. For better sampling, the scanning speed must be at least twice with that of the input frequency.

3.4 DESIGN OF D FLIP-FLOP

Flip-flops are the conventional memory elements used to realize synchronous logic circuits. They hold the state of a clock cycle machine to the next. They are also used to step feedback in a cyclic logic circuit to prevent the logic from having racing state or vibration. It is one of the necessary elements in the pipeline ADC, the most important point that increases here, ie it is used as a delayelement that the bits of the all-phase are synchronized by configuring the flip-flop as a varying longitudinal switch registry, It is synchronized the export of pipeline ADC. For example, for 7 bit pipeline ADC, the first phase has the 7-bit shift register in the later phase in length 6 and decreases in the final phase. The other use of this flip-flop is at the end of the generation of the conversion signal,

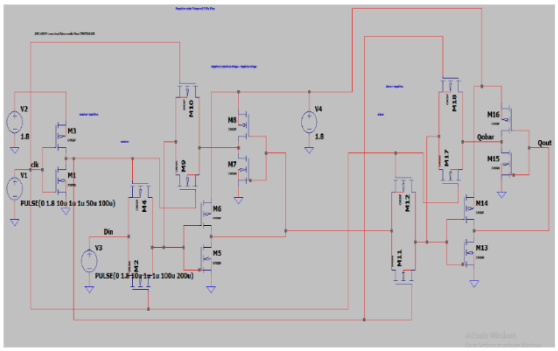

Figure 3.5 Schematic of D-Flip-Flop

Wherein it is configured as a counter that will start counting when the ADC receives the conversion start signal and will stop after seven clock cycles.

3.5 TC To BC Encoder

Encoder converts code 01 to code 1 in a two-level scheme. Code 01 is replaced by code 1outofn by "01" generators. This code is then converted into binary code. shows a single cell optimized "01" oscillator circuit using only four transistors only when the output is at full scale in a small area. In the case of a 6-bit A / D converter, 63 generator cells "01" are used to generate code 1 of 63.

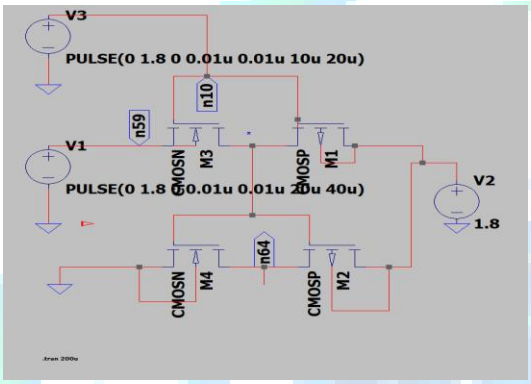

Fig 3.6 Schematic of TC to BC Encoder

Table 3.1: Table For TC To BC Encoder

n59	n10	n64
0	0	0
0	1	0
1	0	1
1	1	0

3.6 DESIGN OF INVERTING GAIN AMPLIFIER

Each pipeline ADC stage have one gain block, whose gain depends on the number of output bits of each stage, Mathematically –

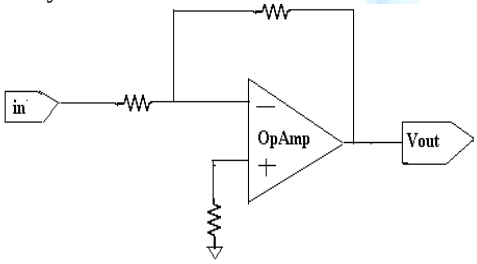

Figure 3.7 Inverting Gain Amplifier Configured For Gain of 4

Where Av is the gain of the amplifier and n is the number of bits for each stage. Therefore, the OPAMP must be configured in closed loop style because the proposed design has only one bit per degree and therefore the required gain is 4. The configuration is shown in Figure 3.9

3.7 SIMULATION RESULTS AND DISCUSSION

The 14 bit ADC pipeline design was done using tsmc018 (Taiwan Semiconductor Corporation) technology, but the ADC pipeline design is limited to 8-bit. This is CADIII LT Spice Switching Tool with 0.18µm in LT opening. Supply voltage - bipolar +/- 1.25 (1.8 V). The following tools were used for the design: LT SPICE SWITCHER CADIII for the circuit, LT for modelling. A DC sweep essentially produces a waveform as the DC input voltage (current) varies from start to finish and the output voltage and current are observed. This DC analysis allows us to know the input signal diversity, DC offset and output swing. In the analysis of alternating current, a 1 volt source is practical, and the frequency of this source is very variable. From this analysis, in principle two plots can be obtained, ie gain and component phase versus frequency. Transient analysis analyzes the time domain analysis of the device. When a signal that is not time-reliable, such as a sinusoidal, square wave, or linear-linear signal, exhibits output voltage or current characteristics such as free load slew rate expected effects. Power analysis and other analyzes can be done with the spice itself.

3.8 RESULTS OF SAMPLE & HOLD

The transient response of the sample &hold circuit shows in Figure 3.8

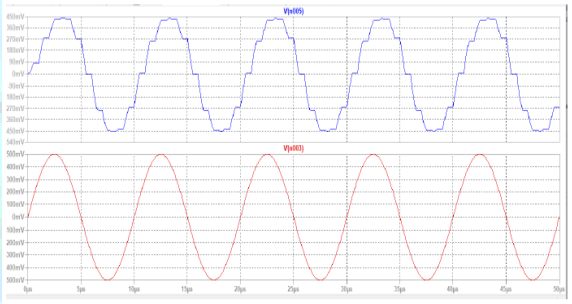

Fig. 3.8. Transient Result Of Sample & Hold Circuit

3.9 RESULTS OF COMPARATOR

The dc breakdown product of comparator, whose reference is set at 0.9 volt. Curve shows output of second stage. Transient results of comparator.

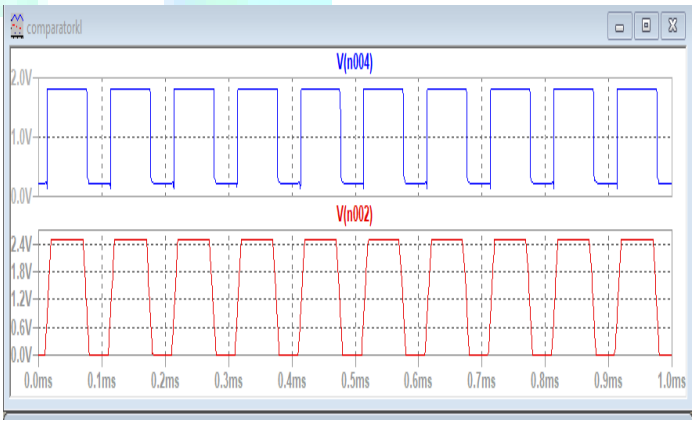

Fig.3.9 Transient Analysis Of Comparator

Results of DAC

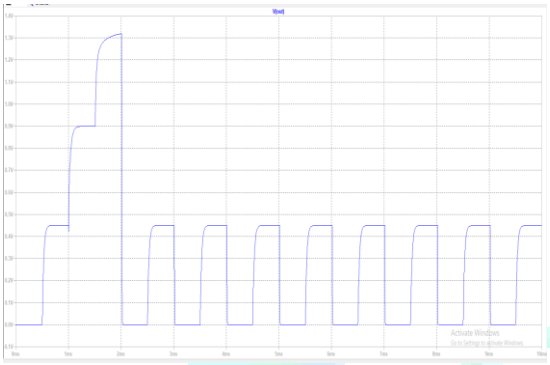

Figure 3.10 Transient Results Of DAC

Results of D-Flip flop

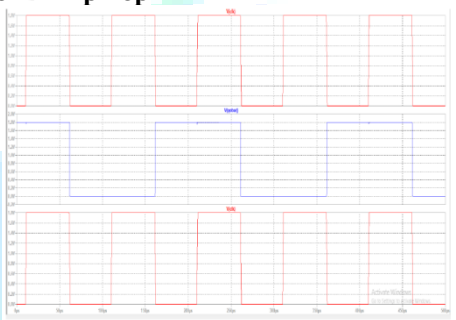

Figure3.11 Transient Result of D-Flip-flop

Results of TC-T0- BC Encoder The transient response of the tc to bc Encoder results is shown in Figure 3.12

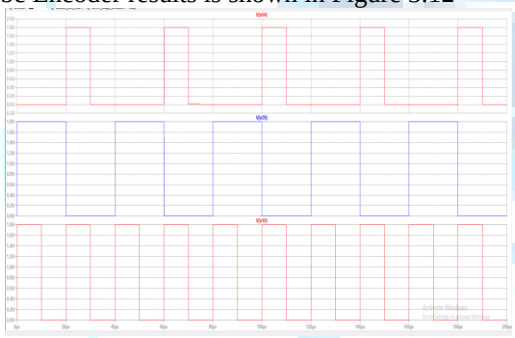

Figure 3.12 Transient result of TC- TO -BC Encoder

3.10 Implementation of Pipeline ADC

Here we express how the pipelines are implemented by the sub-circulation mentioned above. In the first step for intent of pipeline , we must design sample and holding circuit, 2bit ADC, 2bitDAC, an adder and an inverting amplifier amplifier. What we have designed here will use six phases to get the resolution of 14bit. If we are the input signal for the sample and holding circuit. Get the sampled output and functionally with comparators and receive the digital output that this digital signal applies to a DAC unit to an analog signal, and the output of DAC withdrawn to a sampled output and amplifies through gain amplifier, Furthermore, applied to the second phase. and replicate these steps. 3.10 The 8-phase implementation show Figure 3.8 Temporary response from ADC with sinusoidal input.

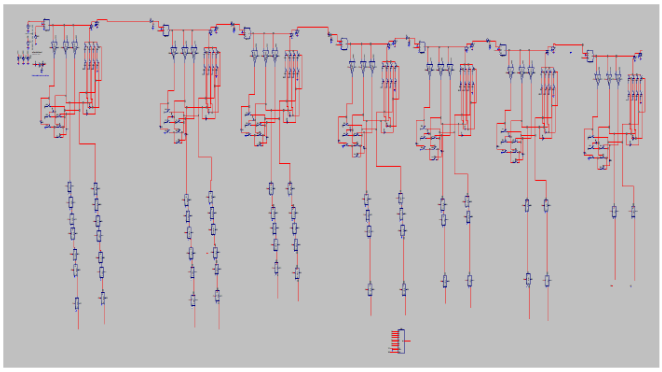

Figure 3.13 Schematic Of 14-Bit Pipeline ADC

3.11 Results of Pipeline ADC :-Presents the plot of 14-bit pipeline ADC with sinusoidal input shown in Figure 3.18

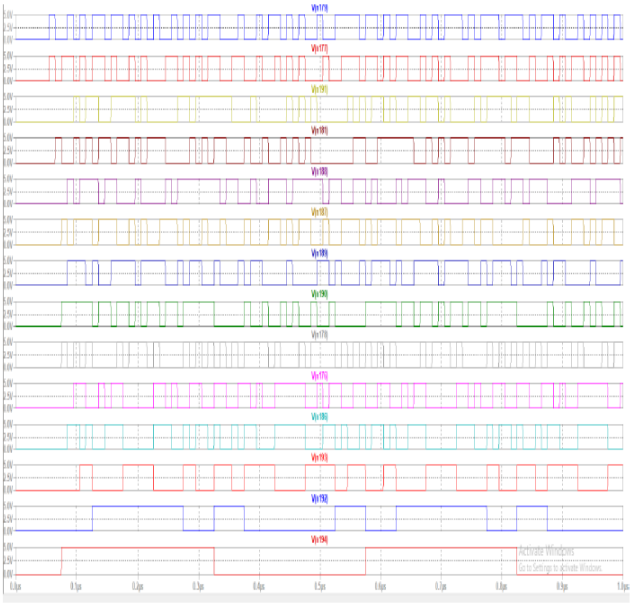

Figure 3.14 Pipeline ADC

Table 3.2 Comparison Of The Earlier Work Done With Proposed Design Results

S.No	Name of Parameters	Earlier work done [5]	Proposed design
1	Resolution	12bit	14bit
2	comparator	7	3
3	Sampling frequency	20MHz	40MHz
4	Gain	68dB	77dB
5	Power dissipation		3.7mW
6	technology	65nm	0.18µm
7	Power supply	1.8V	1.8V

V. CONCLUSION AND FUTURE WORK

A. Conclusions

The design of 14-bit pipeline ADC is executed in the TSMC 018 µm technology. The design isimplemented in LT SPICE SWICER CAD -III schematic editor, and the results are checked withLT spice and simulation in LT herbs. The key design module is now summarized. 3 TiQcomparator is worn in a single ADC phase. An analog multiplexer is used as a DAC. An OPAMPis used in analog adder.A unit amplifier is designed using an OPAMP for scanning and holding circuit. An analogousadder is designed with OPAMP. The shift register is designed with D flip-flop. The generaldesign is tested with different input signals, and the results are satisfactory for the specification.Due to the convergence problem, which occurs in the tool, only 14-bit design is performed byADC. The 14-bit pipeline ADC uses up to 1 GHz input frequenciesThe thesis presents a comprehensive pipeline ADC design methodology. The pipeline ADC design methodology provides a comprehensive and quantitative mapping matrix between systemlevel ADC performance specs (e.g., power optimization, sampling rate, resolution, input voltage range, etc.) and the critical design parameters at block levels, such as, thermal noise limitation op-amp selection in S/H and MDAC, DC gain and closed-loop gain bandwidth of op-amps requirement, sampling capacitor selection criterion etc.

B. Future Work

Multistage calibration: The calibration techniques discussed in chapter four discussed in Chapter four have only tackled the calibration of the first pipeline stage. Future research could check whether it is feasible about the backend pipeline levels to be easily calibrated with the help of the techniques, which in chapter four and / or a combination of other calibration techniques digital calibration circuit: the shown in chapter four ADC Chapter Four to A MATLAB script to mimic the functionality of digital calibration. In order to complete the examination in fast calibration, ADC can take a study on detailed complexity and power consumption of the digital calibration circuit in various technologies. Integrated S / H technology in multi bit pipeline increments: the proposed technique of eliminating the S / H in Chapter Five with a pipeline ADC in which the first phase was only a phase of 1.5 internship. The proposed technique can also cooperate with multi bit pipeline phases - since multi bit stages have a more closer requirement of the maximum clock slot due to read-end use of the previous S / H removing techniques, an implementation of the proposed technology with a multi bit phase would be attractive. Integrated S / H technology in combination with PGA: In some applications, pipelined ADCs are required from a PGA. If the PGA is a switched capacitor circuit, no front end S / H is required, but the PGA becomes the dominant force of the force. Future studies could see the possibility of using the techniques developed in Chapter Five to eliminate a frontend PGA, but somehow the programming of gain maintaining. 6. Implement topologies in recent technologies: The three prototypes discussed in this work were all implemented in 1.8V, 0.18 µM CMOS. Since the three contributions of this work are primarily at the architectural level, they can also be applied to deeper submicron technologies (eg 65nm, 45nm). It is expected that lower energy consumption can be achieved in recent technologies.

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REFERENCES

[1] A 12-bit 20MS/s 56.3mW Pipelined ADC with Interpolation-Based Nonlinea CalibrationJie Yuan, Member, IEEE, Sheung Wai Fung, Kai Yin Chan, and Ruoyu Xu, Student Member, IEEE 2011

[2] Low-Power Pipeline ADC for Wireless LANs J. Arias, V. Boccuzzi, L. Quintanilla,L. Enríquez, D. Bisbal, M. Banu, and J. Barbollaieee 2004

[3] A 6 BIT 1.2 GSps low power flash ADC IN 0.13um digital cmos Martin claraandreassantnerthamoshartig

[4] A Pipeline Analogue to Digital Converter in 0.35 μ m CMOS S.W. Ross †, StudenTMember, IEEE, and S. Sinha Member, IEEE 2007

[5] A 7 bit 16MS/s low power cmos pipeline ADC Zhuang zhaodong ,lizhiqugieee 2011

[6] Tobias Buckel Peter Preyler Alexander Klinkan DamirHamidovic Christoph Preissl Thomas Mayer Stefan Tertinek Siegfried Brandstaetter Christian Wicpalek Andreas Springer Robert Weigel A Novel Digital-Intensive Hybrid Polar-I/Q RF Transmitter Architecture IEEE Transactions on Circuits and Systems I: Regular Papers Year: 2018DOI: 10.1109/IEEE

[7] PummyRatna Usha P Verma Enhanced Receiver Architecture For Leakage Reduction inWideband EW Transceivers With Overlapping RF And IF 2018 IEEE MTT-S International Microwave and RF Conference (IMaRC) Year: 2018 ISBN: 978-1-5386-8221-0 DOI: 10.1109/IEEE Kolkata, India, India

[8] 8. Ram Sunil Kanumalli Ahmed Elmaghraby Andreas Gebhard Christian Motz Thomas Paireder ; Christina Auer Mario Huemer Mixed-Signal Based Enhanced Widely Linear Cancellation of Modulated Spur Interference in LTE-CA Transceivers 2018 52nd AsilomarConference on Signals, Systems, and Computers Year: 2018 ISBN: 978-1-5386-9218- DOI: 10.1109/IEEEPacific Grove, CA, USA, USA

